

What is claimed is:

1 1. A microprocessor comprising:

2 a first integrated circuit chip having an active face
3 including a central processing unit; and

4 a second integrated circuit chip mounted on, and
5 electrically connected to, the active face of the first
6 integrated circuit, wherein the second integrated circuit chip
7 provides added functionality to the central processing unit of
8 the first integrated circuit.

2. The microprocessor of claim 1, wherein the central
processing unit comprises a digital signal processor.

3. The microprocessor of claim 1, wherein the central
processing unit comprises a field programmable gate array.

4. The microprocessor of claim 1, wherein the second
integrated circuit chip comprises memory.

5. The microprocessor of claim 4, wherein the memory
comprises cache.

6. The microprocessor of claim 4, wherein the memory
comprises DRAM.

1 7. The microprocessor of claim 4, wherein the memory
2 comprises SRAM.

1 8. The microprocessor of claim 4, wherein the memory
2 comprises FLASH.

1 9. The microprocessor of claim 1, wherein the second
2 integrated circuit chip comprises an analog-to-digital
3 converter.

1 10. The microprocessor of claim 1, further comprising a third
2 integrated circuit chip adjacent the second integrated circuit
3 chip wherein the third integrated circuit chip adds further
4 functionality to the integrated circuit microprocessor.

1 11. The microprocessor of claim 1, wherein the electrical
2 connection between the first integrated circuit chip and the
3 second integrated circuit chip is by direct connection of
4 metalizations on the active faces of the first and second
5 integrated circuit chips by a bonding layer.

1 12. The microprocessor of claim 1, wherein the first and
2 second integrated circuit chips are further defined as having

1 a profile, and wherein the profile of the second integrated
2 circuit chip is less than the profile of the first integrated
circuit chip.

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- 1 13. A microprocessor comprising:
- 2 a first chip having an active face including a central
- 3 processing unit; and
- 4 a second chip having an active face, the second chip
- 5 mounted on, and electrically connected to, the active face of
- 6 the first chip, wherein the second chip adds functionality to
- 7 the central processing unit of the first chip and wherein the
- 8 electrical connection is by a bonding layer between
- 9 metalization that is integral with the active faces of the
- 10 first and second chips.
- 1 14. The microprocessor of claim 13, wherein the central
- 2 processing unit comprises a digital signal processor.
- 1 15. The microprocessor of claim 13, wherein the central
- 2 processing unit comprises a field programmable gate array.
- 1 16. The microprocessor of claim 13, wherein the second chip
- 2 comprises memory.
- 1 17. The microprocessor of claim 13, wherein the second chip
- 2 comprises an analog-to-digital converter.

1 18. The microprocessor of claim 13, further comprising a
2 third chip adjacent the second chip wherein the third chip
3 adds further functionality to the integrated circuit
4 microprocessor.

1 19. The microprocessor of claim 13, wherein the first and
2 second integrated circuit chips are further defined as having
3 a profile, and wherein the profile of the second integrated
4 circuit chip is less than the profile of the first integrated
5 circuit chip.

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1 20. A method for creating an integrated circuit
2 microprocessor comprising the steps of:

3 obtaining a first chip with an active surface including
4 a central processing unit having a metalization and a bonding
5 layer;

6 obtaining a second chip having a different functionality
7 from the first chip, the second chip having a metalization and
8 a bonding layer;

9 mounting the second chip on the active surface of the
10 first chip; and

11 electrically connecting the first and second chips by
12 electrically connecting the bonding layers on the
13 metalization.